Amendments to the Specification

ABSTRACT OF THE DISCLOSURE

Please replace the Abstract of the Disclosure with the following paragraph:

In order to estimate the layout area from a logic circuit diagram constituted by a transistor as a minimum unit, there is provided a hierarchy developing unit for developing logic circuit diagram information having a hierarchical information structure at a transistor level, a configuration parameter information extracting unit for extracting information such as gate length, gate width or the like of each transistor, an area calculating unit for calculating each transistor area from the above information using an area calculation formula, and layout area estimating unit for obtaining a layout area by adding all areas of the transistors together.